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EXAMINER	
YEH, EUENG NAN	
ART UNIT	**PAPER NUMBER**
2624	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/840,233	STEVENS, ASHLEY MILES	
	Examiner	Art Unit	
	Eueng-nan Yeh	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,9,10,12-24,28,29,31-43,47,48 and 50-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9,10,12-24,28,29,31-43,47,48 and 50-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

FINAL ACTION

Response to Amendment

1. The following Office Action is responsive to the amendment and remarks received on September 24, 2007. Original claims 6-8, 11, 25-27, 30, 44-46, and 49 were canceled. Claims 1-5, 9-10, 12-24, 28-29, 31-43, 47-48, and 50-57 remain pending. In response to the amendment, the previous specification and claim "objections" are withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 10, 12, 15-18, 20-24, 29, 31, 34-37, 39-43, 48, 50, and 53-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Ogoro (GB 2 345 774 A), Kim et al. (U.S. 2003/003128 A1), and Lavelle (U.S. 2003/0179208 A1).

Regarding claims 1, 20, and 39, Ogoro discloses an image processing system:

initial processing stage of said processing operation on said at least one data block (as depicted in figure 1, numeral 4 is the digital signal processor, DSP, "a DSP for performing various digital signal arithmetic processing operations in accordance with an arithmetic processing request" page 5, line 23; "In the initial state such as a power-on state, a predetermined frequency corresponding to an arithmetic processing amount in the DSP 4 is instructed from the clock frequency calculation unit 7 to the clock generator 8..." page 7, line 27);

deriving from at least one result of said initial processing stage a complexity measure indicative of an amount of data processing required to perform at least one further processing stage of said processing operation upon said at least one data block (as depicted in figure 1, numeral 6 the arithmetic processing amount estimation unit is the complexity measure, "the arithmetic processing amount estimation unit 6 estimates the current arithmetic processing amount in the DSP 4..." page 8, line 12);

setting said performance controlling parameter to a predicted value in dependence upon said complexity measure (as depicted in figure 1, numeral 7 calculate the performance controlling parameter, clock frequency, in dependence upon numeral 6 the complexity measure, numeral 8 is the clock generator to set up said performance controlling parameter; see also page 8, lines 9-24); and

performing said at least one further processing stage upon said at least one data block subject to said predicted value of said performance controlling parameter (as depicted in figure 1, numeral 8 the newly calculated clock frequency, i.e. the predicted

performance controlling parameter, will feed to numeral 4 to process next data input; see also figure 4 the transition of frames processed from clock speed S_0 to S_1);
at least one of said plurality of data blocks of said input data stream comprises one of an image field or an image frame (image frame as depicted in Ogoro figure 4).

Ogoro does not explicitly disclose one or more features to derive complexity measure and counts as one complexity measure. Furthermore, Ogoro does not teach a deferred rendering graphics processor.

Kim, in the same field of endeavor of "video and image coding" in paragraph 5, line 1, teaches many features for the complexity measure: "complexity measure in accordance with one embodiment of the present invention is relatively invariant with the quantization parameter (QP) ... the bit count for non-texture information, such as frame headers/syntax and motion vectors ..." in paragraph 111, line 2, see also "The complexity measure $C_{g,i}$ addresses both the motion and texture bit count ... " in paragraph 113, line 1. Furthermore, "to obtain a constant or consistent quality within each GOV or GOP, it is preferable to allocate the bit budget according to frames within each GOV or GOP based on frame complexity and while still meeting buffer constraints" in Kim paragraph 135, line 4. Kim also teaches " the present invention can be used with a variety of video compression standards, such as, by way of example, the MPEG-4 standard, as well as MPEG-1, MPEG-2..." in paragraph 34, line 7.

It would have been obvious at the time the invention was made to one of ordinary skill in the art to have the data processing system Ogoro made with the complexity measure as taught by Kim, in order not only the complexity measure uses bit count and

can be derived from more features but also to "provides efficient error resiliency by selectively and adaptively encoding macroblocks in a predicted frame" in Kim paragraph 16, line 2.

The Ogoro and Kim combination does not explicitly teach a deferred rendering graphics processor.

Lavelle, in the same field of endeavor of computer graphics ("a graphics computing system configured to dynamically adjust a number of rendering passes to achieve a targeted quality constrain" in paragraph 3, line 2), teaches "[t]he graphics rendering system may defer sample filtering till just before the display buffer swap. The entire scene is filtered at the animation rate (which depends on scene complexity)" in paragraph 193, line 1. Furthermore Lavelle teaches the Z buffer operation: "hidden surface removal may cause some of the samples rendered earlier in the scene to be replaced by samples rendered later in the scene ... A cluttered scene with many objects in front of each other, as seen from the eye point, will have a higher depth complexity" in Lavelle paragraph 252, line 6.

It would have been obvious at the time the invention was made to one of ordinary skill in the art to have the image data processing system Ogoro and Kim made with list from deferred rendering processor as taught by Lavelle, in order to "dynamically adjust a number of rendering passes to achieve a targeted quality constrain" in Lavelle paragraph 3, line 3.

Regarding claims 2, 21, and 40, said performance controlling parameter is at least one of a processor frequency and a processor operating voltage of said data processing apparatus (as depicted in Ogoro figure 1, numeral 7 "A clock frequency calculation unit for calculating a new frequency of the clock to be supplied to the DSP 4..." at Ogoro page 6, line 14; the processor frequency is the performance controlling parameter).

Regarding claims 3, 22, and 41, said complexity measure is also derived in dependence upon a result of a processing operation performed on at least one preceding data block of said input data stream (as depicted in Ogoro figure 1, numeral 6 is the complexity measure, "numeral 6 denotes an arithmetic processing amount estimation unit for estimating an arithmetic processing amount in the DSP 4 on the basis of information from the controller 5" at Ogoro page 6, line 11).

Regarding claims 4, 23, and 42, said result of said processing operation on said preceding data block is a processing time ("In this embodiment, all tasks issued to the DSP 4 must be completed within a frame having a predetermined period of time" at Ogoro page 7, line 8).

Regarding claims 5, 24, and 43, said complexity measure is scaled in dependence upon said result of said processing operation on said preceding data block to derive a value for said performance controlling parameter ("The arithmetic processing

amount is assumed to be proportional to the product of the arithmetic processing speed and time" at Ogoro page 7, line 14. To simplify the explanation, set variable A be the arithmetic processing amount, and T be the time to process A, then the predicted process time T' for next block of data A' is: $T' = (A' / A) T$. Thus the complexity measure T' is scaled by A'/A and the clock frequency calculation unit (Ogoro figure 1, numeral 7) needs to be adjusted accordingly).

Regarding claims 10, 29, and 48, said performance controlling parameter is at least one of a processor frequency and a processor operating voltage of a graphics co-processor (as depicted in Ogoro figure 1, numeral 7 the clock frequency calculation unit is the performance controlling parameter calculation unit, therefore, "a clock having a new frequency is supplied to the DSP 4" page 8, line 23. The Digital Signal Processor "performs various signal processing operation" at Ogoro page 1, line 14 and graphics co-processor can be one of processors).

Regarding claims 12, 31, and 50, said one or more features used to derive said complexity measure include texture formats associated with said constituent image elements (discussed in claims 7, 26, and 45, complexity measure includes texture formats).

Regarding claims 15, 34, and 53, said performance controlling parameter is set by estimating a number of memory accesses per said one of an image field or an image

frame in view of said derived complexity measure (as discussed in claims 2, 20, and 39, bit count is used for the complexity measure and the number of RAM accesses is proportional to the bit counts).

Regarding claims 16, 35, and 54, said one of an image field and an image frame is MPEG encoded and said complexity measure is a number of motion vectors required to decode said one of an image field or an image frame (discussed in claims 1, 20, and 39, the image frame is MPEG encoded).

Regarding claims 17, 36, and 55, said predicted value of said performance controlling parameter (as depicted in Ogoro figure 1, numeral 7 is the performance controlling parameter unit) is selected from a predetermined range of parameter values ("the frequency of the clock supplied from the clock generator *(Ogoro figure 1, numeral 8)* to the DSP is controlled on the basis of an arithmetic processing amount in the DSP" at Ogoro page 5, line 15; this is to say that the selection (figure 1, numeral 8) is limited to arithmetic processing amount which is predetermined by the system's central processing unit).

Regarding claims 18, 37, and 56, said predicted value of said performance controlling parameter is set in dependence upon at least one of a target processing time and a target power consumption level ("present invention relates to a DSP "Digital Signal Processor" control apparatus and method and, more particularly, to a DSP

control apparatus and method capable of reducing DSP power consumption" at Ogoro page 1, line 5).

4. Claims 19, 38, and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Ogoro, Kim, and Lavelle as applied to claims discussed above, and further in view of Gawne et al. (U.S. 5,420,787).

Regarding claims 19, 38, and 57, Ogoro discloses ways to define processing frequency and then to adjust the processing power consumption.

Ogoro does not explicitly disclose what to do when target processing time or target power consumption level cannot be met.

Gawne, in the same field of endeavor of signal analysis ("The present invention relates to the field of neuron signal analysis" at column 1, line 7), teaches ways to set up priority order during process. "low priority operations are performed only if sufficient computing power is available after the high and medium priority operations" at column 6, line 19.

It would have been obvious at the time the invention was made to one of ordinary skill in the art to include the data processing system of Ogoro, Kim, and Lavelle combination, to include the priority schema taught by Gawne such that major and important features can be captured when the predicted processing time or power cannot be met.

5. Claims 9, 13, 28, 32, 47, and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Ogoro, Kim, and Lavelle combination as applied to claims 1, 20, and 39 discussed above, and further in view of Jeddeloh (U.S. 6,252,612 B1).

Regarding claims 9, 28, and 47, Ogoro, Kim, and Lavelle combination disclose many features for complexity measure. Ogoro, Kim, and Lavelle combination does not explicitly disclose 3-D image elements.

Jeddeloh, in the same field of endeavor of computer graphics ("a computer system having a second memory controller including an accelerated graphics port" at column 1, line 18), teaches a computer system architecture: "enable relocation of a portion of the 3D graphics data, such as the texture data, from the local frame buffer to main memory ... moving 3D graphics data to a memory controller with its main memory, the architecture of the invention reduces the total system cost" at column 8, lines 12-25. Jeddeloh further teaches the importance of this accelerated graphics port to handle conditions such as:

a) 3-D data: "the emergence of high-bandwidth applications, such as three dimensional (3D) graphics applications, threatens to overload the PCI bus" at column 1, line 40;

b) screen resolution: "to transfer an average 3D scene (polygon overlap of three) in 16-bit color at 30 frames/sec at 75 Hz screen refresh, estimated bandwidths of 370 megabytes/sec to 840 megabytes/sec are needed for screen resolutions from 640X480 resolution (VGA) to 1024X768 resolution (XGA)" at column 1, line 56.

It would have been obvious at the time the invention was made to one of ordinary skill in the art to have the image data processing system of Ogoro, Kim, and Lavelle combination, can handle three dimensional graphics features as taught by Jeddeloh, in order to have a proper computer system architecture with accelerated graphic port to avoid 3-D graphics applications with the "threatens to overload the PCI bus" at Jeddelph column 1, line 42.

Regarding claims 13, 32, and 51, said one or more features used to derive said complexity measure comprises a screen resolution associated with said one of an image field or an image frame (discussed in claims 9, 28, and 47, Ogoro, Kim, and Lavelle combination does not explicitly disclose screen resolution).

Jeddeloh also teach the importance of image process and screen resolution.

It would have been obvious at the time the invention was made to one of ordinary skill in the art to include the image data processing system of Ogoro, Kim, and Lavelle combination with screen resolution as complexity measure as taught by Jeddeloh, for the reason that "rendering of 3D graphics on a display requires a large amount of bandwidth..." Jeddeloh column 1, line 62.

6. Claims 14, 33, and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Ogoro, Kim, and Lavelle as applied to claims 1, 20, and 39 discussed above.

Regarding claims 14, 33, and 52 the combination of Ogoro, Kim, and Lavelle disclose many features to comprise the complexity measure.

The combination of Ogoro, Kim, and Lavelle does not explicitly disclose the step of graphics processing enable/disable.

As discussed in claims 1, 20, and 39, Kim also teaches "Optionally, in high noise environment, the macroblock bit allocation process can be disabled or not used so that the decoder can assume that the QP *(quantization parameter)* is the same for each macroblock" in paragraph 152, line 1. This disable/enable graphics processing feature can affect the complexity measure.

It would have been obvious at the time the invention was made to one of ordinary skill in the art to have the image data processing system of Ogoro, Kim, and Lavelle combination with graphics processing features enable/disable function as taught by Kim, in order not only to have a more complete complexity measure but also to "prevent the decoder from using the wrong QP when portions of a frame have been corrupted or lost" in Kim paragraph 152, line 4.

Response to Arguments

7. Summary of Applicant's Remark:

The previous specification and claim objections should be withdrawn in view of the amendment.

Examiner's Response:

Examiner agrees, and the previous objections are withdrawn.

8. *Summary of Applicant's Remarks*:

"Kim neither discloses nor suggests the use of any complexity measure for the purpose of setting a performance controlling parameter of a data processing apparatus" at response page 18, line 3 from bottom..

Examiner's Response:

It is the combination of Ogoro, Kim, and Lavelle teaches the setting of performance controlling parameters. Refer to the rejections above.

9. *Summary of Applicant's Remarks*:

"Furthermore, the Examiner is believed to be utilizing impermissible hindsight in his argument that a skilled person would combine various portions of the Kim, Ogoro and Lavelle references in order to arrive at the subject matter of amended claim 1 which incorporates claim 11" at response page 19, line 13.

Examiner's Response:

The combination of Ogoro, Kim, and Lavelle is for image processing error resiliency and quality assurance. Refer to the rejections above.

Conclusion

10. Applicant's amendment is rejected in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eueng-nan Yeh whose telephone number is 571-270-1586. The examiner can normally be reached on Monday-Friday 8AM-4:30PM EDT.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vikkram Bali can be reached on 571-272-7415. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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